System-Level Programming

17 µC System Architecture – Peripherals

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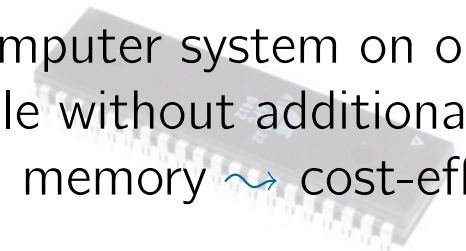
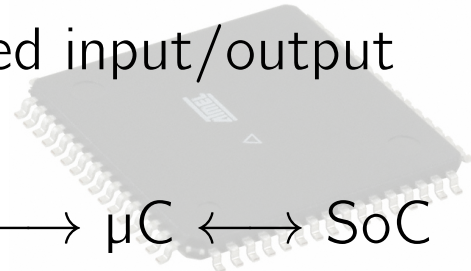
http://sys.cs.fau.de/lehre/ss25

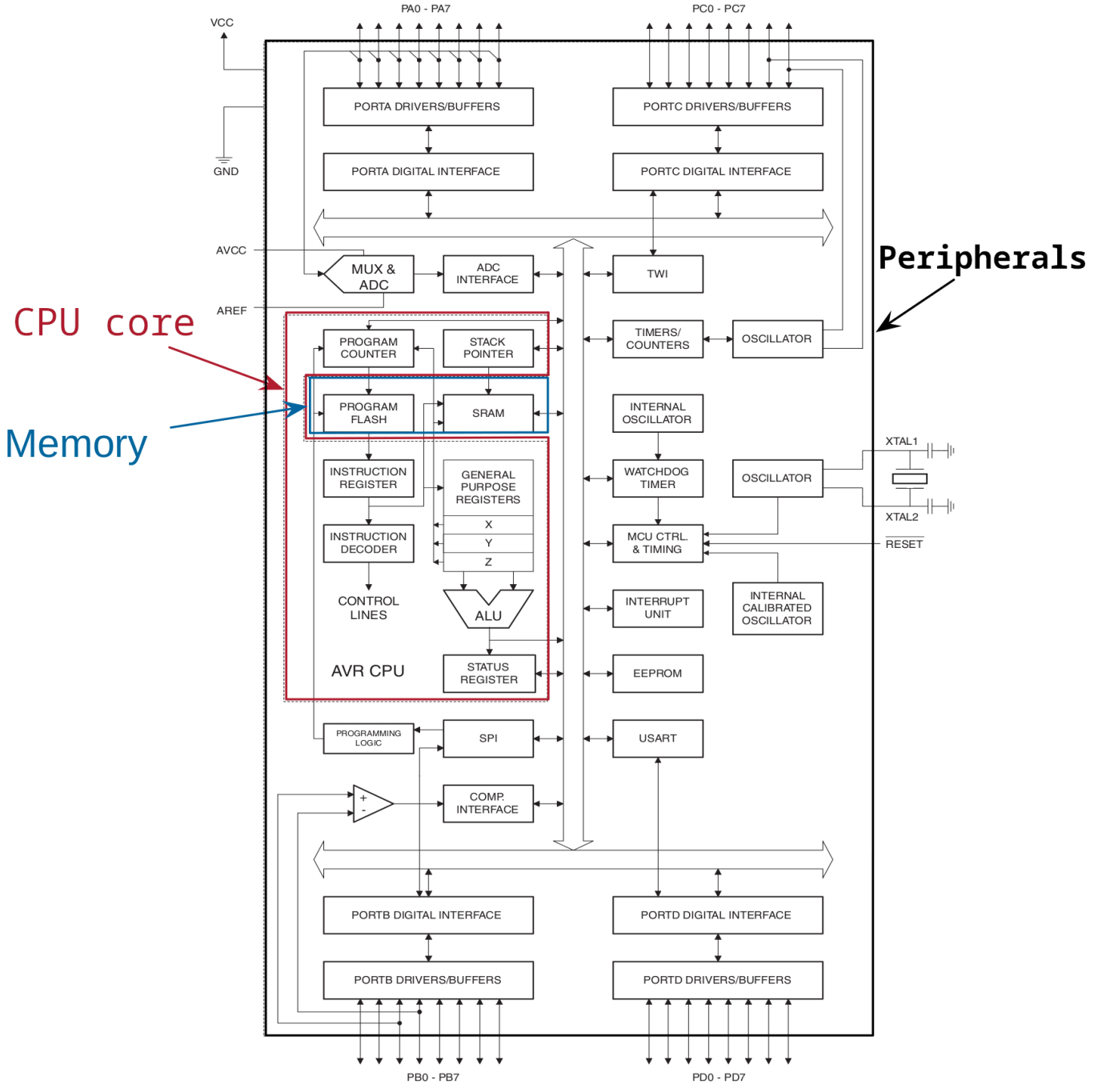
What is a µController?





- **µController** := processor + memory + **peripherals**
  - in fact, computer system on one chip $\longrightarrow$ *System-on-a-Chip* (SoC)
  - often usable without additional external components, like e. g., timers and memory $\rightsquigarrow$ cost-efficient system design
- main features are (plentiful) integrated input/output components (peripherals)
- distinctions are not fixed: processor $\longleftrightarrow$ µC $\longleftrightarrow$ SoC
  - AMD64 CPUs also have included timers, memory (cache), ...
  - some µC execute at speeds close to "large processors"

Example ATmega32: Block Circuit Diagram



Peripheral Devices

- **peripheral device:** hardware component that is located "outside" of the central unit of a computer
  - traditional (laptop): keyboard, monitor, ...
    ($\mapsto$ physically "outside")
  - in general: hardware functions that are not directly mapped into the processor's instruction set
    ($\mapsto$ logically "outside")
- peripheral components are addressed via I/O registers
  - control registers: instructions to control/query state of peripheral is encoded by bit patterns (e. g., `DDRD` for ATmega)
  - data registers: required for exchange of data
    (e. g., `PORTD`, `PIND` for ATmega)
  - registers are often only available as *read-only* or *write-only*

Peripheral Devices: Examples

- typical peripheral devices of µControllers
  - **timer/counter** — counting registers that are incremented with a defined frequency (timer) or by external signals (counter) and that trigger an interrupt at a configurable counting value.
  - **watchdog timer** — timer that has to be written to regularly otherwise a RESET is triggered (“dead man’s button”).
  - **(a)synchronous serial interface** — component for serial (bit-wise) exchange of data with a synchronous (e. g., RS-232) or asynchronous (e. g., I^2C) protocol.
  - **A/D converter** — component for one-time/continuous discretization of voltage values (e. g., 0–5V $\mapsto$ 10-bit integer).
  - **PWM generators** — component for generating pulse-width–modulated signals, pseudo-analog (D/A) output.
  - **ports** — groups of usually 8 ports which can be set to GND or Vcc and whose states can be monitored. ↪ 17–12
  - **bus systems** — SPI, RS-232, CAN, Ethernet, MLI, I^2C, . . .

Peripheral Devices – Registers

- different architectures for accessing I/O registers
  - memory-mapped: (most µC) — Registers are integrated into address space; access with memory instructions of the processor (`load`, `store`)
  - port-based: (x86-based laptops) — Registers are organized in a separate I/O address space; access with special `in`- and `out`-instructions

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- addresses of the registers are listed in the hardware's documentation

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	8
$3E ($5E)	SPH	–	–	–	–	SP11	SP10	SP9	SP8	11
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
$3C ($5C)	OCR0	Timer/Counter0 Output Compare Register								86
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	67
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	67
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	68

[1]

Peripheral Devices – Registers (continued)

- for every port x, three registers are defined (example for $x = D$)

- **DDRx** **Data Direction Register:** Determines for every pin i whether it is used as input (bit i=0) or output (bit i=1).

7	6	5	4	3	2	1	0
DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- **PORTx** **Data Register:** If pin i is configured to be an output, bit i determines the voltage level (0=GND sink, 1=Vcc source). If pin i is configured to be an input, bit i activates the internal pull-up resistor (1=active).

7	6	5	4	3	2	1	0
PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- **PINx** **Input Register:** Bit i represents the voltage level at pin i (1=*high*, 0=*low*), independent of the data direction of the register.

7	6	5	4	3	2	1	0
PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Examples: ↪ 3–7 and ↪ 3–11 [1]

Peripheral Devices – Registers (continued)

- Memory-mapped registers enable convenient access
  - register $\mapsto$ memory $\mapsto$ variable
  - all C operators are directly available (e. g., `PORTD++`)
- Syntactically, preprocessor macros simplify the access:

```
#define PORTD (*(volatile uint8_t *)   0x12    )
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`(*(volatile uint8_t *)  0x12  )`: address: volatile uint8_t *(cast ↪ 7–19)

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`(volatile uint8_t *)0x12`: address: volatile uint8_t *(cast ↪ 7–19)

`*(volatile uint8_t *)0x12`: value: volatile uint8_t (dereferencing ↪ 13–4)

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`(volatile uint8_t *)0x12`: `address: volatile uint8_t *` (cast ↪ 7–19)

`*(volatile uint8_t *)0x12`: `value: volatile uint8_t` (dereferencing ↪ 13–4)

Therefore `PORTD` is syntactically-equivalent to a `volatile uint8_t`-variable that is stored at address `0x12`.

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Therefore `PORTD` is syntactically-equivalent to a `volatile uint8_t`-variable that is stored at address `0x12`.

- Example

```
#define PORTD (*(volatile uint8_t *) 0x12)

PORTD |= (1<<7);           // set D.7
uint8_t *pReg = &PORTD;    // get pointer to PORTD
*pReg &= ~(1<<7);          // use pointer to clear D.7
```

Access to Registers and Concurrency

- Peripheral devices operate concurrently to the software
  ⇝ Value in hardware registers can change anytime
- This change in contrast to the assumption of the compiler
  - Access to variables only takes place by the currently executed function
    ⇝ Variables are temporarily stored in registers

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```
// C code
#define PIND \
    (*(uint8_t*) 0x10)
void foo(void) {
    ...
    if (! (PIND & 0x2)) {

        // button0 pressed
        ...
    }
    if (! (PIND & 0x4)) {

        // button 1 pressed
        ...
    }
}
```

```
// Resulting assembly code

foo:
   lds   r24, 0x0010 // PIND->r24
   sbrc  r24, 1      // test bit 1
   rjmp L1
   // button0 pressed
   ...
L1:
   sbrc r24, 2       // test bit 2
   rjmp  L2

   ...
L2:
   ret
```

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```

PIND is not again loaded from memory. The compiler assumes the value in r24 to still be accurate.

Details of Assembly Instructions

- knowledge how to program assembly instructions not necessary [1]
- however, semantics of assembly instructions necessary for *understanding concurrency*
- `lds`
  - load direct s from SRAM
  - load variable from memory to a register (for operations)
- `sbrc`
  - skip if bit in register cleared
  - test condition, depending on condition's result, skip following instruction
- `rjmp`
  - relative jump
- `ret`
  - return address is popped from the stack
  - return from a function call

The `volatile` Type Modifier

- **Solution:** declare variable as `volatile` (*"transient, changeable"*)
  - Compiler minimizes the time, the variable is held in registers
    - ⇝ value is read *immediately before* use
    - ⇝ value is written *immediately after* modification

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```

```
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   // button0 pressed
   ...
L1:
   lds  r24, 0x0010 // PIND->r24
   sbrc r24, 2      // test bit 2
   rjmp L2

...
L2:
   ret
```

`PIND` is declared as `volatile`. It is therefore loaded from memory before each test.

The `volatile` Type Modifier (continued)

- `volatile` semantics prevent many code optimizations;
  in particular the removal of apparently unnecessary code
- `volatile` can be used to implement active waiting:

```
// C code                                    // Resulting assembly code
void wait(void) {                            wait:
    for(uint16_t i=0; i<0xffff; i++);            // compiler has optimized
                                                 // "unneeded" loop
}                                                ret
```

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- `volatile` can be used to implement active waiting:

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```

`volatile`!

```
// Resulting assembly code
wait:
    // compiler has optimized
    // "unneeded" loop
    ret
```

Attention: volatile $\mapsto$ **$$$**

The use of `volatile` causes considerable runtime penalties

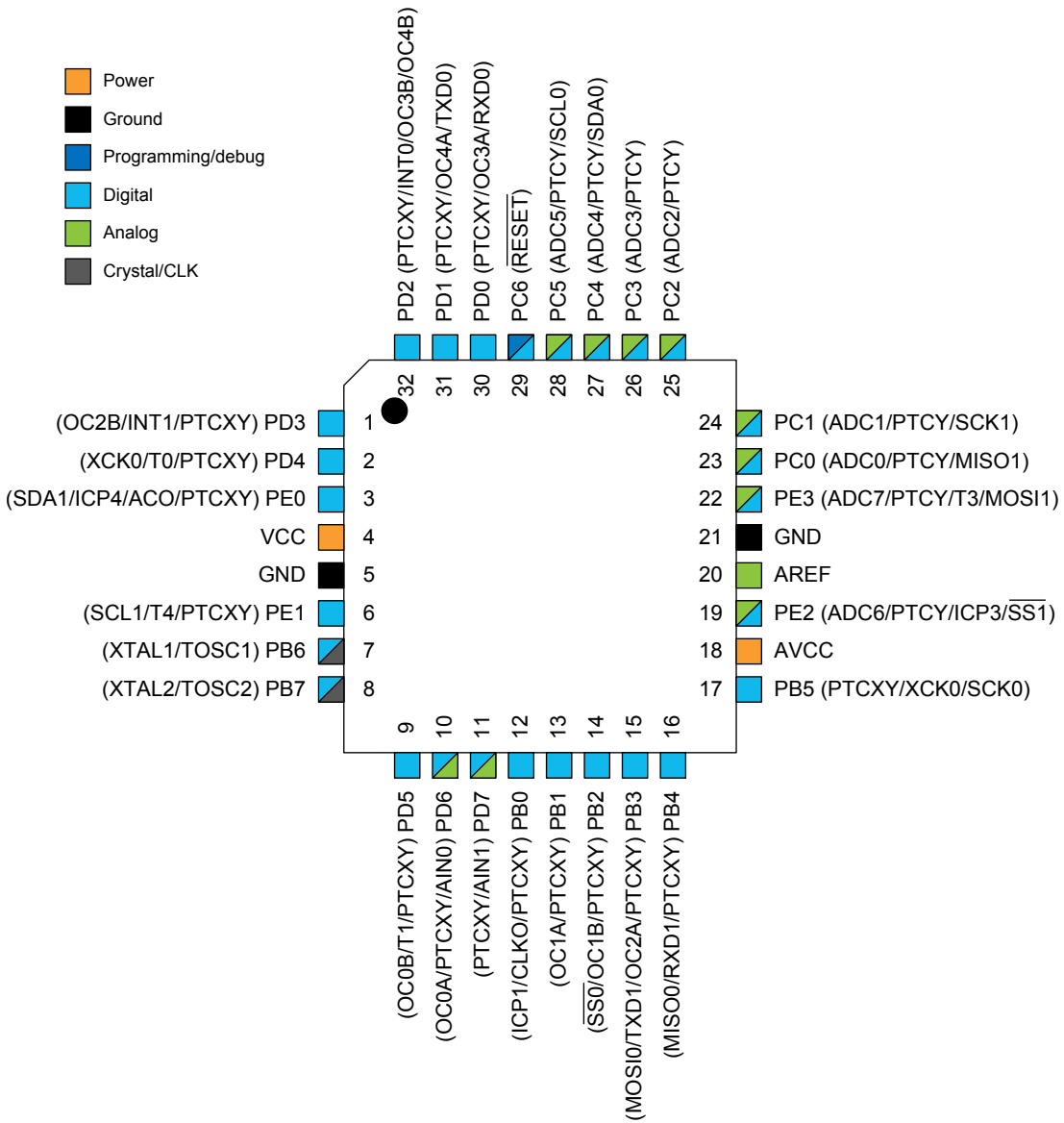
- Values cannot be stored in registers any longer
- Most code optimizations cannot be performed any longer

Rule: Use `volatile` only in **justified scenarios**

Peripheral Devices: Ports

- **Port** := group of (usually 8) digital inputs/outputs
  - Digital output: bit value $\mapsto$ voltage level at µC pin
  - Digital input: voltage level at µC pin $\mapsto$ bit value
  - External interrupt: voltage level at µC pin $\mapsto$ bit value
    (on voltage change) $\rightsquigarrow$ processor executes interrupt program
- This function is usually configurable per pin
  - Input
  - Output
  - External interrupt (only for some inputs)
  - Alternative functions (pin used by another device)

Example ATmega328PB: Port/Pin Assignment



For reasons of cost efficiency nearly every pin is assigned twice. The configuration of the respective functionality takes place in software.

E. g., pins 23–24 are configured as ADCs at the SPiCBoard to connect potentiometer and photo sensor.

Those pins are therefore not available for PORTC.

References

[1] *ATmega328PB 8-bit AVR Microcontroller with 32K Bytes In-System Programmable Flash*. Atmel Corporation. Okt. 2015. URL: https://sys.cs.fau.de/extern/lehre/ss25/spic/uebung/spicboard/Atmel-42397-8-bit-AVR-Microcontroller-ATmega328PB_Datasheet.pdf.